IN THE CLAIMS

Please amend the claims as follows.

For the Examiner's convenience, a list of all claims is included below.

1. (Original) A memory device comprising:

a first subarray of memory cells organized into rows and columns;

a first plurality of bit lines, each coupled to a column of memory cells;

a first set of subarray isolators to selectively couple the first plurality of bit lines to a first row of sense amplifiers;

a first set of common isolators to selectively couple the first row of sense amplifiers to a plurality of global I/O lines; and

isolator control logic to coordinate the operation of the first set of common isolators to allow data received from outside the memory device and present on the plurality of global I/O lines to be latched by the first row of sense amplifiers, to store an indication that the data latched by the first row of sense amplifiers is dirty, to coordinate the operation of the first set of subarray isolators to allow data latched by the first row of sense amplifiers to be written back to a row of memory cells within the first subarray, and to remove an indication that the data latched by the first row of sense amplifiers is dirty.

2. (Original) The memory device of claim 1, further comprising:

a second subarray of memory cells organized into rows and columns;

a second plurality of bit lines, each one of the second plurality of bit lines being coupled to a column of memory cells;

a second set of subarray isolators to selectively couple the second plurality of bit lines to a second row of sense amplifiers, wherein the second set of subarray isolators are operable by the

isolator control logic to allow data latched in the second row of sense amplifiers to be written back to a row within the second subarray by allowing the second row of sense amplifiers to transmit data through both the second set of subarray isolators and the second plurality of bit lines and to the row within the second subarray when there is an indication that the data latched in the second row of sense amplifiers is dirty; and

a second set of common isolators to selectively couple the second row of sense amplifiers to the plurality of global I/O lines, wherein the second set of common isolators is operable by the isolator control logic to allow data received from outside the memory device and present on the plurality of global I/O lines to be latched by the second row of sense amplifiers, and wherein the isolator logic stores an indication that the data latched by the second row of sense amplifiers is dirty.

3. (Original) The memory device of claim 1, further comprising:

a first bank of memory comprised of the first and second subarrays, the first and second set of subarray isolators, the first and second set of sense amplifiers, and the first and second sets of common isolators; and

a second bank of memory.

4. (Original) The memory device of claim 1, further comprising control logic configured to receive a mini write command and to respond by operating at least the first set of common isolators to cause data to be copied from the global I/O lines and through the first set of common isolators to the first row of sense amplifiers where the data is latched, and storing an indication that the data latched in the first row of sense amplifiers is dirty.

5. (Original) The memory device of claim 4, wherein the control logic is further configured to receive a writeback command and to respond by operating at least the first set of subarray isolators and a row of memory cells within the first subarray to cause data latched by the first

row of sense amplifiers to be copied from the first row of sense amplifiers, through both the first set of subarray isolators and the first plurality of bit lines, and the row of memory cells.

6. (Original) The memory device of claim 1, wherein the control logic is further configured to receive a mini row activate command wherein a row address identifying a row within the first subarray is received by the control logic to signal that data latched within the first row of sense amplifiers from the row within the first subarray is to be transmitted through the first set of common isolators to the plurality of global I/O lines upon receipt of a read command.

7. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of both rows of memory cells and rows of sense amplifiers within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device,

wherein the control logic transmits a mini write command to the memory device to cause data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells has been copied to the specific row of sense amplifiers and the specific row of memory cells is the open row within the bank.

8. (Cancelled)

9. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of both rows of memory cells and rows of sense amplifiers within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device

~~The controlling device of claim 7~~, wherein the control logic transmits a mini row activate command and a mini write command to the memory device to cause the specific row of memory cells to become the open row within the bank and to cause data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells has been copied to the specific row of sense amplifiers and the specific row of memory cells is not the open row within the bank.

10. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of both rows of memory cells and rows of sense amplifiers within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device ~~The controlling device of claim 7~~,

wherein the control logic transmits a row activate command and a write command to the memory device to cause the specific row of memory cells to become the open row within the bank, to cause the data in the specific row of memory cells to be copied to the specific row of sense amplifiers, and to cause the data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells have not been copied to the specific row of sense amplifiers and the current contents of the specific row of sense amplifiers are not dirty.

11. (Currently Amended) A controlling device comprising:

a first storage location in which data concerning the status of both rows of memory cells and rows of sense amplifiers within a bank of memory cells within a memory device is stored;

control logic coupled to the first storage location to check data within the first storage location to determine if the contents of a specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device ~~The controlling device of claim 7~~,

wherein the control logic transmits a writeback command, a row activate command and a write command to the memory device to cause the specific row of sense amplifiers to writeback the data currently latched within the specific row of sense amplifiers to the other row to which that data corresponds, to cause the specific row of memory cells to become the open row within the bank, to cause the data in the specific row of memory cells to be copied to the specific row of sense amplifiers, and to cause the data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells have not been copied to the specific row of sense amplifiers and the current contents of the specific row of sense amplifiers are dirty.

12. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows;

a memory controller coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row to which data is to be written in response to a request from the processor to write data is already cached by a specific row of sense amplifiers, to check if the specific row is the open row within the bank, and to check if the data cached by the specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device.

wherein the memory controller transmits a mini row activate command and a mini write command to the memory device to cause the specific row of memory cells to become the open row within the bank and to cause data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells has been copied to the specific row of sense amplifiers and the specific row of memory cells is not the open row within the bank.

13. (Cancelled)

14. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows;

a memory controller coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row to which data is to be written in response to a request from the processor to write data is already cached by a specific row of sense amplifiers, to check if the specific row is the open row within the bank, and to check if the data cached by the specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device ~~The computer system of claim 12~~,

wherein the control logic transmits a row activate command and a write command to the memory device to cause the specific row of memory cells to become the open row within the bank, to cause the data in the specific row of memory cells to be copied to the specific row of sense amplifiers, and to cause the data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells have not been copied to the specific row of sense amplifiers and the current contents of the specific row of sense amplifiers are not dirty.

15. (Currently Amended) A computer system comprising:

a processor;

a memory device having at least one bank in which a plurality of memory cells are organized into rows;

a memory controller coupled to the processor and having a first storage location that the memory controller accesses to determine if the contents of a specific row to which data is to be written in response to a request from the processor to write data is already cached by a specific row of sense amplifiers, to check if the specific row is the open row within the bank, and to check if the data cached by the specific row of sense amplifiers is dirty; and

a memory bus coupling the control logic to the memory device to allow commands to be transmitted from the control logic to the memory device ~~The computer system of claim 12~~,

wherein the control logic transmits a writeback command, a row activate command and a write command to the memory device to cause the specific row of sense amplifiers to writeback the data currently latched within the specific row of sense amplifiers to the other row to which that data corresponds, to cause the specific row of memory cells to become the open row within the bank, to cause the data in the specific row of memory cells to be copied to the specific row of sense amplifiers, and to cause the data transmitted to the memory device to be latched by the specific row of sense amplifiers, if the current contents of the specific row of memory cells have not been copied to the specific row of sense amplifiers and the current contents of the specific row of sense amplifiers are dirty.

16. (Original) A method comprising:

determining whether or not the contents of a specific row of memory cells within a subarray of memory cells organized into multiple rows and columns are already cached within a specific row of sense amplifiers;

determining whether or not the specific row of memory cells is the open row of a bank of a memory device in which the subarray is located;

determining whether or not the data currently cached in the specific row of sense amplifiers is dirty;

transmitting data to the memory device;

transmitting a mini write command to the memory device to write the data transmitted to the memory device to at least a portion of the specific row of sense amplifiers if the contents of the specific row of memory cells have been copied to the specific row of sense amplifiers, the specific row of memory cells is the open row of the bank of the memory device.

17. (Original) The method of claim 16, further comprising transmitting a mini row activate command to the memory device to cause the specific row of memory cells to become the open row of the banks of the memory device if the contents of the specific row of memory cells have been copied to the specific row of sense amplifiers, but the specific row of memory cells is not the open row of the bank of the memory device.

18. (Original) The method of claim 16, further comprising:

transmitting a writeback command to the memory device to cause a set of subarray isolators to permit the current contents of the specific row of sense amplifiers to be written back to the other row of memory cells to which those contents correspond, if the contents of the specific row are not cached in the specific row of sense amplifiers and the current contents of the specific row of sense amplifiers are dirty; and

transmitting a row activate command to the memory device to make the specific row the open row of the bank of the memory device, if the contents of the specific row are not cached in the specific row of sense amplifiers.

19. (Original) A method comprising:

operating a first set of isolators coupled to a first row of sense amplifiers in response to the receipt of a mini write command to allow data received on a set of global I/O coupled to the input of a memory device of which the first row of sense amplifiers are a part to be copied into and latched by the first row of sense amplifiers;

storing an indication that the data latched by the first row of sense amplifiers is dirty; and

operating a second set of isolators coupled between a first set of bit lines and the first row of sense amplifiers in response to the receipt of a writeback command to allow the data latched by the first row of sense amplifier to be copied to and stored in a first row of memory cells also coupled to the first set of bit lines.

20. (Original) The method of claim 19, further comprising operating the first set of isolators to isolate the first row of sense amplifiers from the set of global I/O lines while allowing data received on the set of global I/O lines to be copied into and latched by a second row of sense amplifiers without data stored within the first row of sense amplifiers being lost.

21. (Original) A machine-accessible medium comprising code that when executed by a processor within an electronic device, causes the electronic device to:

check whether or not a memory device is capable of caching the contents of a row of memory cells within a row of sense amplifiers, and whether or not the memory device is capable of responding to a writeback command;

program a memory controller to transmit a mini row activate command to activate a row of which the contents have been determined to have been cached within a row of sense amplifiers to make possible the subsequent writing of data to the row of sense amplifiers; and

program a memory controller to transmit a mini write command to write data to the row of sense amplifiers and store an indication that the data latched in the row of sense amplifiers is dirty in lieu of writing the data to the row of memory cells being cached by the row of sense amplifiers.

22. (Original) The machine-accessible medium of claim 21, further causing the electronic device to transmit a precharge command causing the row of sense amplifiers to be isolated from bit lines that otherwise couple the row of sense amplifiers to columns of memory cells within a subarray while the precharge operation to precharge the bit lines is carried out so as to prevent data cached within the row of sense amplifiers from being lost.